Jordan University of Science and Tech
Department of Electrical Engineering
EE420 Second Exam
2nd semester 03/04 Dr. O. Qasaimeh

Q1) (8 Points)

For the ECL circuit shown in Fig. 1 if $\beta = 50$, $V_{BE} = 0.6\ V$ and $V_{Ref} = 1.0\ V$, find

a) The low and high input voltages.

b) When A = High and B = Low, find the current passing through R_{C1}

c) Find R_{C1}.

d) When A = Low and B = Low, find collector voltage of Q_2

e) Modify the circuit to build an OR gate.

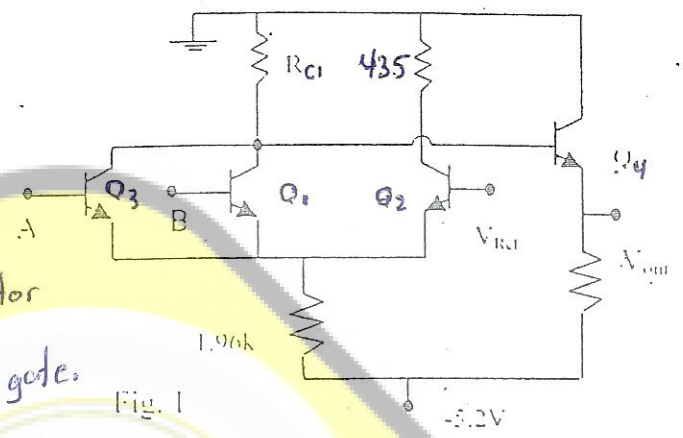

Fig. 1

Q2) (8 Points)

For the circuit shown in Fig. 2, if $V_T = 0.8\ V$, $K_1 = K_2 = 10^{-3}\ A/V^3$ and $K_L = 1.5 \times 10^{-4}\ A/V^2$.

a) When A = 0 V and B = 0 V, find the output voltage (V_{out}).

b) " A = High and B = Low, find V_{out}.

c) " A = High and B = High, find V_{out}.

d) Modify the circuit to build a NAND gate using CMOS.

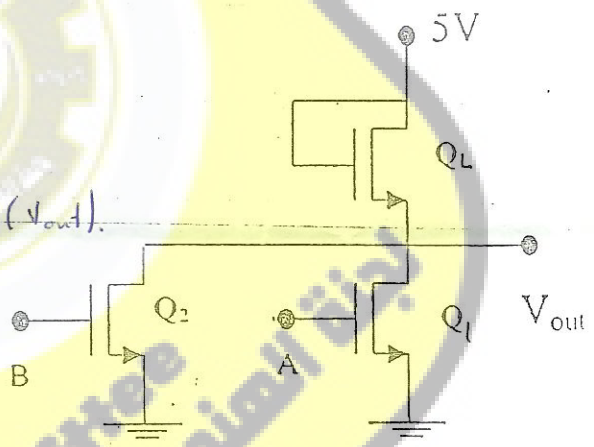

Fig. 2

Q3) (9 points)

For the circuit show in Fig. 3 if $\beta = 50$ and

a) Plot $V_{B2}(t)$, $V_{C2}(t)$ and $V_{C1}(t)$ and with the help of these figures explain the operation of the circuit.

b) Find R_x and R_c which produces an output pulse having a pulse width of 0.22 ms. Assume that the min. period for the trigger is 0.3ms.

c) Find the pulse amplitude ($|V_{out}|$) in volt.

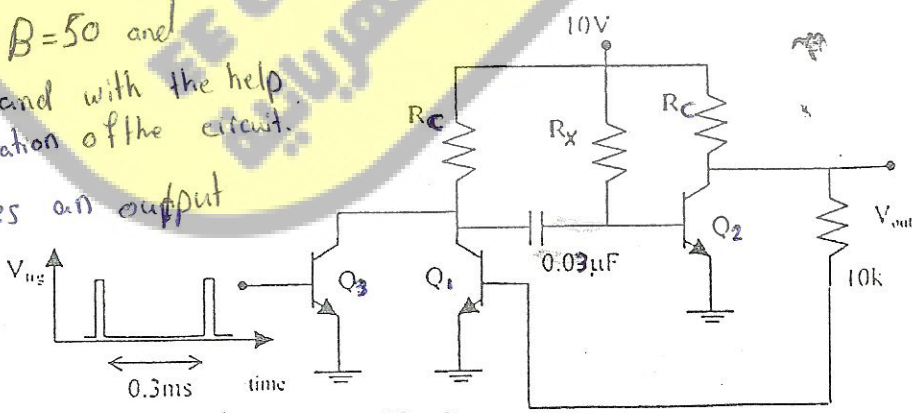

Fig. 3